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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,727	NING, XIAN JIE	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *11-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/773,727. Currently, claims 1-19 are pending.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 17-19, drawn to a process of making, classified in class 438, subclass 381.

II. Claims 11-16, drawn to a product, classified in class 257, subclass 528.

3. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process. For example, in the current invention, each of a plurality of openings formed in a first insulating layer are filled entirely with a metal layer, and a surface of the metal layer is planarized to form the vertical metal structures in the claimed product. In another and materially different fabrication process,

the vertical metal structures in the claimed product can be formed by selectively depositing a metal layer in each of the plurality of openings.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Richard Ogawa on 09 March 2005 a provisional election was made without traverse to prosecute the invention of I, claims 1-10 and 17-19. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-16 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

6. The drawings are objected to because: the drawings to do not show dielectric layer 105 overlying insulating film 103 as indicated in the specification (see page 8, lines 1-5), the reference number "203" does not refer to a surface of the metal layer as indicated in the specification (see page 8, lines 27-28, and the reference number "601" does not refer to a capacitor dielectric layer as indicated in the specification (see page 9, line 16).

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference numbers mentioned in the description: metal material "107" (see page 8, line 5), first insulating material "109" (see page 8, line 14), plurality of openings "111" (see page 8, lines 17 and

19), barrier layer "121" (see page 8, line 21), and a second metal layer "603" (see page 9, line 20).

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference numbers not mentioned in the description: "117" (see fig. 1).

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The disclosure is objected to because of the following informalities: "to" should be --do-- (page 2, line 10), "occupying" should be --occupy-- (page 3, line 8), "structure" should be --structures-- (page 3, line 10), "florinated" should be --fluorinated-- (page 8, line 2), "occupying" should be --occupies-- (page 8, line 26). Appropriate correction is required.

10. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

11. Claims 1-10 and 17-19 are objected to because of the following informalities: "structure" should be "structures" (claim 1, line 12 and claim 17, line 16), and "filing" should be "filling" (claim 7, line 2). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. *Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The following claim language recited in claim 1 lacks antecedent basis: "the dielectric material" (line 6), "the capacitor insulating layer" (line 18), and "the barrier layer structures" (line 19).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application

designated the United States and was published under Article 21(2) of such treaty in the English language.

13. *Claims 1-3, 5, 8, 10, and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al. (US 6,593,185 B1).*

The Tsai et al. patent (Tsai '185) discloses a method for manufacturing integrated circuit devices including capacitor structures (figs. 2-10 and accompanying text). The method comprises the following process steps, as in claims 1 and 17: providing a semiconductor substrate 10 (fig. 2 and col. 4, lines 38-43); forming an overlying thickness of first insulating material 18 on the semiconductor substrate (fig. 2 and col. 4, lines 45-49); defining a capacitor region and an interconnect region (fig. 3 and col. 4, lines 59-64); forming a plurality of openings 26 within the thickness of the first insulating material and the capacitor region of the first insulating material, each of the openings including a width and a height (fig. 3 and col. 4, lines 59-64); forming a plurality of openings 22, 24 within the thickness of first insulating material in the interconnect region (fig. 3 and col. 4, lines 59-64); forming a barrier layer 28 overlying an exposed surface of each of the plurality of openings in the capacitor region and the interconnect region (fig. 4 and col. 4, line 64 - col. 5, line 4); filling each of the openings with a metal material, the metal material occupying substantially an entire region of each of the openings to form a plurality of metal structures 30, 32, each of the metal structures having a width and height (fig. 4 and col. 5, lines 4-11); planarizing a surface region of each of the metal structures (fig. 4 and col. 5, lines 12-16); patterning the

capacitor region to expose the barrier layer on each of the metal structures to form an opening within the capacitor region excluding the plurality of metal structures and barrier layer, the plurality of metal structures and barrier layer forming a first electrode structure of a capacitor (fig. 5 and col. 5, lines 18-23); forming an insulating layer 46 overlying each of the exposed barrier layer structures to form a capacitor dielectric for the capacitor (fig. 6 and col. 5, lines 23-34); filling the opening within the capacitor region using a second metal layer 50 overlying the capacitor insulating layer to form a second electrode structure of the capacitor (fig. 7 and col. 5, lines 40-43); and planarizing the second metal layer (fig. 8 and col. 5, lines 44-47).

The metal structures comprise substantially copper material, *as recited in claim 2* (col. 5, lines 4-11).

In one disclosed embodiment, the insulating layer 46 is silicon nitride, as *recited in claim 3* (col. 5, lines 27-29).

The method further comprises forming a dual damascene interconnect structure within the first insulating material concurrently with one or more of the steps of forming the integrated circuit, *as recited in claim 5* (col. 4, lines 59-64).

The patterning comprises selective removal of a portion of the first insulating material to expose the plurality of metal structures, *as recited in claim 8* (col. 5, lines 18-23).

The integrated circuit is a mixed mode signal device, *as recited in claim 10* (col. 4, lines 1-6).

The second metal layer 50 comprises a copper material, *as recited in claim 18* (col. 5, lines 40-43).

The metal material is copper fill material, *as recited in claim 19* (col. 5, lines 4-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai '185.*

Tsai '185 lacks anticipation of maintaining the insulating layer at a temperature below 400°C, *as recited in claim 4.* However, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to maintain the insulating layer at a temperature below 400°C, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

15. *Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai '185 in view of Tsai et al. (US 6,638,830 B1).*

As explained previously, Tsai '185 discloses forming a barrier layer overlying an exposed surface of each of a plurality of openings in the capacitor region and the interconnect region, and filling each of the openings with a metal material. However, Tsai '185 does not teach that the barrier metal layer comprises tantalum nitride, *as recited in claim 6.* In contrast, the Tsai et al. patent (Tsai '830) discloses a method for manufacturing integrated circuit devices including capacitor structures (see figs. 1-7 and accompanying text), wherein the method comprises forming a barrier layer 26 overlying an exposed surface of each of a plurality of openings in a capacitor region and an interconnect region (fig. 3 and col. 2, line 66 - col. 3, line 8), and filling each of the openings with a metal material 28 (fig. 3 and col. 3, lines 7-12). The method further comprises planarizing a surface region of each of the metal structures (fig. 4 and col. 3, lines 12-19), and patterning the capacitor region to expose the barrier layer on each of the metal structures (fig. 5 and col. 3, lines 19-27). The multilayer barrier layer comprises tantalum nitride (col. 3, lines 1-8).

Both Tsai '185 and Tsai '830 are from the same field of endeavor, fabrication processes for devices in very large-scale or ultra large-scale integrated circuits. Thus, the purpose for which Tsai '830 is relied upon would

have been recognized in Tsai '185 by one of ordinary skill in the art at the time the invention was made.

Again, the metal material 30, 32 in Tsai '185 is copper. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Tsai '185 by forming the barrier layer 28 comprising tantalum nitride, as taught by Tsai '830, since tantalum nitride prevents diffusion of atoms from the metal material 30, 32 into first insulating material 18 (Tsai '830 - col. 3, lines 1-8).

16. *Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai '185 in view of Ning (US 6,451,667 B1).*

As explained above, Tsai '185 discloses the steps of: patterning the capacitor region to expose the barrier layer on each of the metal structures to form an opening within the capacitor region, forming an insulating layer overlying each of the exposed barrier layer structures, filling the opening within the capacitor region using a second metal layer overlying the insulating layer, and planarizing the second metal layer. However, Tsai '185 does not teach that the second metal layer comprises tungsten, *as recited in claim 7.* Ning, on the other hand, teaches forming a second metal layer comprising tungsten in a method for manufacturing integrated circuit devices including capacitor structures (figs. 2-6 and accompanying text). The method comprises: patterning a capacitor region to expose metal structures 124, thereby forming an opening 130 within the capacitor region (fig. 4 and col. 4, lines 58-60),

forming an insulating layer 134 overlying each of the metal structures (fig. 4 and col. 4, lines 61-64), filling the opening within the capacitor region using a second metal layer 136 overlying the insulating layer (fig. 5 and col. 5, lines 5-8), and planarizing the second metal layer (fig. 6 and col. 5, lines 12-15). In one embodiment, the second metal layer, which forms an electrode in a metal-insulator-metal (MIM) capacitor, comprises tungsten (W) (col. 5, lines 5-8). In an alternate embodiment, the second metal layer comprises copper (col. 5, lines 8-11).

Both Tsai '185 and Ning are from the same field of endeavor, fabrication processes for devices in very large-scale or ultra large-scale integrated circuits. Thus, the purpose for which Ning is relied upon would have been recognized in Tsai '185 by one of ordinary skill in the art at the time the invention was made.

The second metal layer 50 in the Tsai '185 patent forms an electrode in a MIM capacitor. As stated above with respect to claim 18, the second metal layer 50 comprises copper. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Tsai '185 by using tungsten in place of copper for the second metal layer 50, as taught by Ning, since tungsten is an alternate conductive material suitable for capacitor electrodes in MIM capacitors.

17. *Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (pat. '185) in view of Wolf et al. ("Dry Etching for VLSI Fabrication," Silicon Processing for the VLSI Era - Vol. 1 Process Technology).*

As explained above with respect to claim 8, Tsai '185 teaches that the patterning step comprises selective removal of a portion of the first insulating material 18 to expose the plurality of metal structures. However, Tsai '185 does not teach that the selective removal uses an etchant selected from C_4F_8, CO, 0_2, CF_4N_2, $ArSF_6$, CHF_3, CH_3F, C_4F_6, and C_2F_6.

In one embodiment, the first insulating material 18 in the Tsai '185 patent comprises silicon dioxide (Tsai '185 - col. 4, lines 45-49). Wolf et al. (Wolf) teaches the use of CHF_3 and C_2F_6 for etching silicon dioxide in a dry etching process (page 550, lines 12-15).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Tsai '185 by using either CHF_3 or C_2F_6 for the selective removal of the first insulating material 18 comprising silicon dioxide, as taught by Wolf, since both CHF_3 and C_2F_6 are selective to silicon dioxide.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
16 March 2005

Mary Wilczewski
Primary Examiner